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09/588,072	06/05/2000	Ahmed Saifuddin	QCPA000320	8110

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	13

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/588,072	SAIFUDDIN ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on January 28, 2003. These drawings are accepted.

Response to Amendment

2. Applicant's arguments with respect to newly added claims 9-34 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 9-34 objected to because of the following informalities:

- Claim 9 cites, "A method" in the preamble. 37 CFR § 1.75 requires that the specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery". The limitations in claim 9 appear to be a list of arbitrary method steps. The Examiner suggests the following preamble: A method for recovery of corrupted bits in a frame (see Top of Page 1 of the Applicants' disclosure).
- Claim 9 cites, "the inner quality metric, wherein the outer quality metric being used for protection of the plurality of information bits and the inner quality metric being used for protection of the at least one group of

information bits". The Examiner suggests the following language to correct grammatical problems: the inner quality metric, the outer quality metric being used for protection of the plurality of information bits and the inner quality metric being used for protection of the at least one group of information bits (i.e., delete wherein).

- Claims 10-15 depend from claim 9.
- Claim 16 also cites, "A method" in the preamble.
- Claims 17-19 depend from claim 16.
- Claim 20 also cites, "A method" in the preamble.
- Claims 21-23 depend from claim 20.
- Claim 24 cites, "An apparatus" in the preamble. The limitations in claim 9 appear to be a list of arbitrary apparatus components. The Examiner suggests the following preamble: An apparatus for recovery of corrupted bits in a frame (see Top of Page 1 of the Applicants' disclosure).
- Claims 25-29 depend from claim 24.
- Claim 30 also cites, "An apparatus" in the preamble.
- Claim 31 depends from claim 30.
- Claim 32 cites, "A system" in the preamble. The limitations in claim 9 appear to be a list of arbitrary system components. The Examiner suggests the following preamble: A system for recovery of corrupted bits in a frame (see Top of Page 1 of the Applicants' disclosure).

- Claims 33 and 34 depend from claim 32.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 9-20 and 22-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kashida, Motokazu et al. (US 4779276 A, hereafter referred to as Kashida) in view of Wright, David A. (US 6445702 B1).

Preliminary Note:

The Examiner asserts that the Authoritative Dictionary of IEEE Standard Terms defines metric as: a value calculated from observed attribute values. The Examiner asserts that digital input data used in an error correction encoder is an observed attribute value since digital input data is an assigned characteristic value of a particular information

value, hence **parity or checksums** generated from an error correction encoder **are metrics** since a parity is a value calculated from the observed attribute values, i.e., the digital input data representing information. Furthermore since errors or lack thereof are indications of the quality of transmission channels within a given system, **parity or checksums** generated from an error correction encoder **are quality metrics** by the dictionary definition of the words. Hence, by the dictionary definition of the words: **inner parity or inner checksums are inner quality metrics and outer parity or outer checksums are outer quality metrics**.

35 U.S.C. 103(a) rejection of claims 9 and 24.

Kashida teaches a method and apparatus comprising: receiving a plurality of information bits (Mapping Coding Circuit 40 in Figure 11 in Kashida is a receiving unit for a plurality of information bits); determining an outer quality metric in accordance with the plurality of information bits (Outer Code Encoding Circuit 43 in Figure 11 in Kashida produces an outer check code from a plurality of information bits comprising the information matrix of Figure 1 of Kashida; Note: the outer check code is an outer quality metric, see Preliminary Note, above) and an inner quality metric in accordance with at least one group of information bits contained in the plurality of information bits (Inner Code Encoding Circuit 44 in Figure 11 in Kashida produces an inner check code from a row which is a group information bits which is an inner quality metric, see Preliminary Note, above); and forming a block comprising the plurality of information bits, the outer quality metric, and the inner quality metric (Figure 9 in Kashida and col. 10, lines 6-19

teach the forming of blocks including the inner and outer quality metrics), wherein the outer quality metric being used for protection of the plurality of information bits (col. 10, lines 6-19 in Kashida teach that the outer code is provided as protection for each information bit along the columns of the matrix in Figure 9) and the inner quality metric being used for protection of the at least one group of information bits (col. 10, lines 6-19 in Kashida teach that the inner code is provided as protection for each information bit along the rows of the matrix in Figure 9, hence is provided as protection for at least one group of information bits).

However Kashida, does not explicitly teach that the block of data in Figure 9 of Kashida is a frame, that is, that the entire error correction block or error correction unit is also a frame.

Wright, in an analogous art, teaches a block error correction unit which includes inner and outer parity code whereby the entire error correction block or error correction unit is also a frame. The Examiner would like to point out that Wright teaches that the error correction block is formed into a frame to avoid complex processing at the transmission side (col. 1, lines 25-45), hence one of ordinary skill in the art at the time the invention was made would be highly motivated to combine the patents since Wright teaches that the error correction block is formed into a frame and Kashida teaches the specifics of a block error correction code with both an inner and outer code required by the Kashida patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kashida with the teachings of Wright by employing error

correction blocks or error correction units that are also frame units. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that employing error correction blocks or error correction units that are also frame units would have provided the opportunity to avoid complex processing at the transmission side (col. 1, lines 25-45).

35 U.S.C. 103(a) rejection of claims 10-13 and 25-28.

Col. 4, lines 59-67 of Kashida teaches the use of cyclic codes (Note: a CRC code is a systematic cyclic code, i.e., a cyclic parity code, as taught in Kashida).

35 U.S.C. 103(a) rejection of claim 14.

See Figure 1, Wright. Outer Code Error Detecting-Correcting Decoding Circuit 55 in Kashida teaches a means for determining whether the frame has been correctly received based on the outer quality metric contained in the frame.

35 U.S.C. 103(a) rejection of claim 15.

Kashida and Wright teach that, if the frame has not been received correctly, determining whether the at least one group of information bits has been received correctly based on the inner quality metric contained in the frame (Inner Code Error Detecting-Correcting Decoding Circuit 55 in Kashida teaches a means for determining whether the at least one group of information bits has been received correctly based on the inner quality

metric contained in the frame); and recovering the at least one group of information bits if the inner quality metric indicates that the at least one group of information bits has been received correctly (Inner Code Error Detecting-Correcting Decoding Circuit 55 in Kashida teaches a means for recovering the at least one group of information bits if the inner quality metric indicates that the at least one group of information bits has been received correctly).

35 U.S.C. 103(a) rejection of claims 16, 20 and 30.

Kashida and Wright teach a method comprising: receiving a frame comprising an outer quality metric and an inner quality metric (Reproducing Part 53 of Kashida is a receiving means for receiving a frame comprising an outer quality metric and an inner quality metric), the outer quality metric being used to verify whether the frame has been received correctly and the inner quality metric being used to verify whether a corresponding group of information bits contained in the frame has been received correctly (see col. 4, lines 59-67 of Kashida, Note: both the inner and outer codes of Kashida are error correcting and detecting codes); and recovering information contained in the frame including the corresponding group of information bits if it is determined that the frame has been correctly received as indicated by the outer quality metric (Outer Code Error Detecting-Correcting Decoding Circuit 58 in Kashida teaches a means for recovering information contained in the frame including the corresponding group of information bits if it is determined that the frame has been correctly received as indicated by the outer quality metric); and recovering the corresponding group of

information bits if it is determined that the frame has not been received correctly as indicated by the outer quality metric but the corresponding group of information bits has been correctly received as indicated by the inner quality metric (Outer Code Error Detecting-Correcting Decoding Circuit 58 in Kashida teaches a means for recovering the corresponding group of information bits if it is determined that the frame has not been received correctly as indicated by the outer quality metric but the corresponding group of information bits has been correctly received as indicated by the inner quality metric).

35 U.S.C. 103(a) rejection of claims 17 and 31.

Kashida and Wright teach determining whether the frame has been received correctly by checking the outer quality metric (Outer Code Error Detecting-Correcting Decoding Circuit 58 in Kashida teaches a means for determining whether the frame has been received correctly by checking the outer quality metric); and if the frame has not been received correctly as indicated by the outer quality metric, determining whether the corresponding group of information bits has been correctly received by checking the inner quality metric (Inner Code Error Detecting-Correcting Decoding Circuit 55 in Kashida teaches a means for determining whether the corresponding group of information bits has been correctly received by checking the inner quality metric, if the frame has not been received correctly as indicated by the outer quality metric).

35 U.S.C. 103(a) rejection of claims 18 and 19.

Col. 4, lines 59-67 of Kashida teaches the use of cyclic codes (Note: a CRC code is a systematic cyclic code, i.e., a cyclic parity code, as taught in Kashida).

35 U.S.C. 103(a) rejection of claim 22.

Inner Code Error Detecting-Correcting Decoding Circuit 55 in Kashida teaches a means for determining if the corresponding portion of the frame has been correctly received as indicated by the respective inner quality metric, recovering the corresponding portion of the frame.

35 U.S.C. 103(a) rejection of claim 23.

Col. 4, lines 59-67 of Kashida teaches the use of cyclic codes (Note: a CRC code is a systematic cyclic code, i.e., a cyclic parity code, as taught in Kashida).

35 U.S.C. 103(a) rejection of claim 29.

See rejection to claims 14 and 15, above.

35 U.S.C. 103(a) rejection of claims 32-34.

Kashida and Wright teach a system comprising: a transmitter to construct and transmit a frame comprising a plurality of information bits (See Figure 1, Wright), an outer quality metric and an inner quality metric, the outer quality metric being used to protect the plurality of information bits (Outer Code Encoding Circuit 43 in Figure 11 in Kashida produces an outer check code from a plurality of information bits comprising the

information matrix of Figure 1 of Kashida) and the inner quality metric being used to protect a particular portion of the plurality of information bits (Inner Code Encoding Circuit 44 in Figure 11 in Kashida produces an inner check code from a row which is a group information bits which is an inner quality metric); and a receiver to receive and decode the frame (Reproducing Part 53 of Kashida is a receiving means for receiving a frame comprising an outer quality metric and an inner quality metric), the receiver to recover information contained in the frame including the particular portion of the plurality of information bits if it is determined that the frame has been correctly received as indicated by the outer quality metric (Outer Code Error Detecting-Correcting Decoding Circuit 58 in Kashida teaches a means for recovering information contained in the frame including the corresponding group of information bits if it is determined that the frame has been correctly received as indicated by the outer quality metric), the receiver to recover the particular portion of the plurality of information bits if it is determined that the frame has not been received correctly but the particular portion has been correctly received as indicated by the inner quality metric (Outer Code Error Detecting-Correcting Decoding Circuit 58 in Kashida teaches a means for recovering the corresponding group of information bits if it is determined that the frame has not been received correctly as indicated by the outer quality metric but the corresponding group of information bits has been correctly received as indicated by the inner quality metric).

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kashida, Motokazu et al. (US 4779276 A, hereafter referred to as Kashida) and Wright, David A.

(US 6445702 B1) in view of Matsukuma, Hiroshi et al. (US 5905741 A, hereafter referred to as Matsukuma.

35 U.S.C. 103(a) rejection of claim 21.

Kashida and Wright, substantially teaches the claimed invention described in claims 1-20 (as rejected above).

However Kashida and Wright, do not explicitly teach the specific use of discarding a frame.

Matsukuma, in an analogous art, teaches that frames are discarded (col. 2, lines 33-40, Matsukuma). Matsukuma teaches that if the errors in a frame exceed the error correcting capabilities of both the inner and outer error correction means then the data is discarded so that an alternative recovery technique can be applied (col. 2, lines 33-40, Matsukuma, i.e., in Matsukuma using another frame).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kashida and Wright with the teachings of Matsukuma by including an additional step of discarding a frame. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that discarding a frame would have provided the opportunity to apply an alternative recovery technique (col. 2, lines 33-40, Matsukuma, i.e., in Matsukuma using another frame).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133
May 17, 2003